A Graphical Method for the Design of Feedback Networks for Microwave Transistor Amplifiers: Theory and Applications

FELIX PEREZ AND VICENTE ORTEGA

Abstract—A new theory is presented that is very useful for the design of feedback transistor amplifiers, including considerations on stability, gain equalization, and matching. The theory is based on graphical feedback diagrams whose construction rules and practical circuit design techniques are described. The method provides insight into the effects of the feedback network elements and saves computer time and money. Three applications are presented: a tuned neutralized bipolar transistor amplifier; a broad-band medium power MESFET amplifier in the 3.7–4.2-GHz range; and a ultrawide-band matched MESFET amplifier covering the 0.1–12-GHz frequency range.

I. Introduction

THE USE of feedback techniques with bipolar transistor amplifiers up to 1 GHz is well known and has been applied to a variety of amplifiers including CATV broad-band equipment [1], [2].

During recent years, important efforts have been made to extend these techniques to higher frequencies. In 1978, Ulrich reported a 0.01–6-GHz transistor amplifier using negative feedback [3]. Gupta *et al.* described a monolithic amplifier covering the band from dc up to 8 GHz [4]. Recently, Niclas *et al.* have reported design methods and results for GaAs MESFET feedback amplifiers up to 18 GHz, obtaining five or more octave bandwidths [5]. The design procedure in the mentioned papers and others [6] relies upon a known model of the transistor that works up to relatively low frequencies and then doing computer optimization.

In this work we present two graphical methods, closely related, that are an excellent first step for designing feedback amplifier modules. The first method is based on the use of a set of curves of constant $G_{\max}$ and stability factor K, plotted in polar diagrams that lead in a simple way to the configuration and values of the feedback circuit in order to obtain gain equalization and unconditional stability in a broad range of frequencies. The second graphical method pays more attention to obtain flat S_{21} over a wide band, controlling the S-parameters and making easier the input and output amplifier matching. The two methods lead to design values close to the final ones, so that very little computer optimization is needed.

We use commercially available bipolar and field-effect transistors and the graphical method relies on the knowledge of the measured S-parameters.

The basic theory and graphical construction techniques are discussed first in this paper. We, then, describe three possible applications: 1) transistor neutralization; 2) broad-band medium power MESFET amplifiers; 3) ultrawide-band MESFET amplifier modules.

Manuscript received December 5, 1980; revised April 10, 1981. This work was supported in part by the Direccion General de Tecnologia, Ministry of Industry of Spanish Government.

The authors are with the Microwave Department, Universidad Politecnica de Madrid, ETSI de Telecomunicación, Ciudad Universitaria, Madrid-3, Spain.

II. Basic Theory: Feedback Diagrams for $G_{\max}$, K and $|S_{21}|$

Let us consider the parallel feedback circuit shown in Fig. 1. This configuration is easily analyzed using Y-parameters.

Assuming, in a first approximation, that the feedback network parameters Y'_{ij} are negligible compared to the corresponding transistor parameters Y_{ij}, that is to say, $Y'_{ij} \ll Y_{ij}$, except Y'_{12}. Then Rollet's stability factor K and the maximum available gain $G_{\max}$ for the feedback amplifier are given by [7], noting that $g_{ii} = \text{Real}\,(Y_{ii})$

$$K_T = \frac{2g_{11}g_{22} - \text{Real}\left[Y_{21}\cdot(Y_{12}+Y'_{12})\right]}{|Y_{21}\cdot(Y_{12}+Y'_{12})|} \tag{1}$$

$$G_{\max} = \frac{|Y_{21}|}{|Y_{12}+Y'_{12}|}\left[K_T - \sqrt{K_T^2-1}\right], \qquad \text{for } K_T > 1. \tag{2}$$

(The approximations that have been made are very good ones for bipolar transistor and fairly good ones for FET's.)

For a given active device, K_T and $G_{\max}$ are functions of the feedback admittance $Y_{12}^T = Y_{12} + Y'_{12}$. Taking this admittance as a complex variable we can plot in a complex plane a set of constant K_T curves and a family of constant gain $G_{\max}$ for each frequency.

In Appendix I we have shown that constant stability factor curves are ellipses, whose principal construction parameters are indicated in Fig. 2.

In a similar way, constant gain $G_{\max}$ curves are a family of circles (see Appendix I) whose centers and radii are indicated in Fig. 3. The circle's envelope is the ellipse $K_T = 1$.

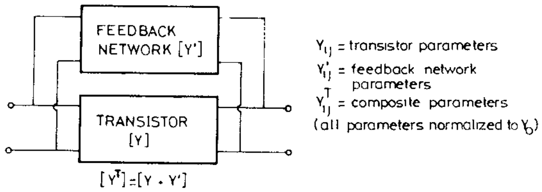


Fig. 1. Parallel feedback network.

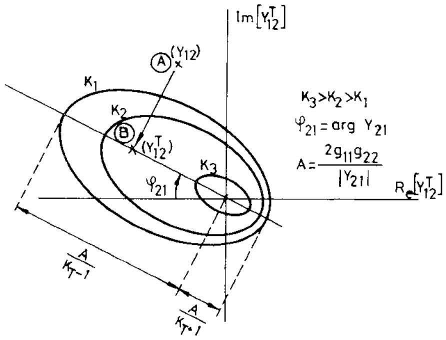


Fig. 2. Constant stability factor K_T curves.

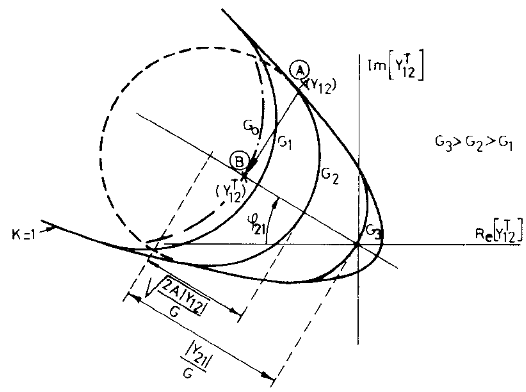


Fig. 3. Constant gain $G_{\max}$ circles.

As a simple application, let us suppose a transistor whose feedback diagrams are those indicated in Figs. 2, 3 for a given frequency, and its Y_{12} is located at point A which is conditionally stable. (This situation occurs for some medium power MESFET in S-band.) If we want to obtain a gain G_0 with unconditional stability, the diagrams clearly indicate that this can be done by translating point A to any other point on the G_0 circle, e.g., point B, and the resulting network is a simple RC series circuits whose values may be calculated from the diagrams.

We can repeat this procedure for several frequencies in a band by plotting the feedback diagram and Y_{12} point at each frequency and then to synthesize the network. This application to broadbanding will be seen in more detail later on.

A little modification has to be done when the approximations made are not valid. If the feedback circuit is reactive the feedback diagrams do not change even if Y'_{11} and Y'_{22} are not negligible. If the feedback circuit includes a resistive part it can be easily shown that the constant K ellipse family suffers a stretching of axis lengths of magnitude given by

$$H=\frac{g_{11}^T g_{22}^T}{g_{11}g_{22}}, \qquad \text{with } g_{ii}^T=\text{Real}\left[Y_{ii}+Y'_{ii}\right] \tag{3}$$

and the constant gain circles are transformed to other circles with the same center and new radii given by

$$R'=R\sqrt{\frac{g_{11}^T g_{22}^T}{g_{11}g_{22}}}=R\sqrt{H}. \tag{4}$$

It is obvious that at first we don't know Y'_{11} and Y'_{22} so we must proceed by trial and error depending on the magnitude of H and R' given by (3) and (4). With those modifications, corrected stability factor K'_T and gain $G'_{\max}$ are given by

$$K'_T=K_T\left[1+\frac{g'_{11}+g'_{22}+g'_{11}\cdot g'_{22}}{g_{11}\cdot g_{22}-\frac{1}{2}\text{Real}\left[Y_{21}\cdot Y_{12}^T\right]}\right] \tag{5}$$

$$G'_{\max}=G_{\max}\frac{K'_T\sqrt{K_T'^2-1}}{K_T-\sqrt{K_T^2-1}}. \tag{6}$$

Our experience shows that two steps in graphical design are enough and the rest of the work is finally done by the computer. It can be shown that resistive components tend to increase stability and to decrease gain.

This graphical method is also valid for feedback series networks by considering the complex plane Z_{12}^T and substituting the Y_{ij} by Z_{ij}, g_{ij} by r_{ij} and so on in all the formulas (1)–(6).

A different approach can be followed if instead of an amplifier of constant $G_{\max}$ we want to use the feedback circuit to obtain an amplifier module with constant S_{21}^T, unconditionally stable and almost matched in a very broad frequency band. In cases where the input or output match is not low enough for some specific application, a balanced stage configuration can be employed.

Let us consider again the circuit shown in Fig. 1. It may be easily shown (see Appendix II) that the network S-parameters are approximately given by

$$\frac{2}{S_{21}^T}\simeq\frac{2}{S_{21}}+Y'_{12} \tag{7.a}$$

$$\frac{2S_{11}^T}{S_{21}^T}\simeq\frac{2S_{11}}{S_{21}}-Y'_{12} \tag{7.b}$$

$$\frac{2S_{22}^T}{S_{21}^T}\simeq\frac{2S_{22}}{S_{21}}-Y'_{12} \tag{7.c}$$

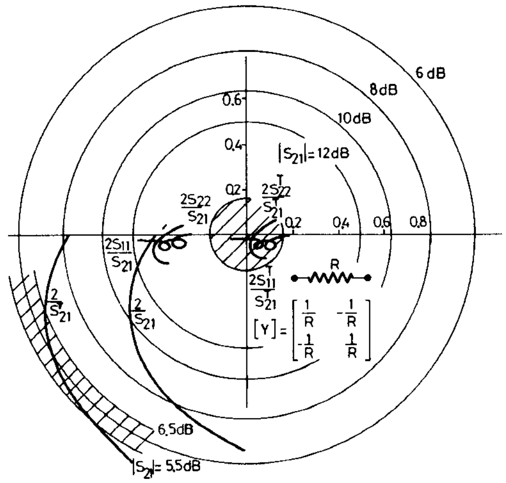


Fig. 4. Feedback diagram for equalization and matching with parallel resistance.

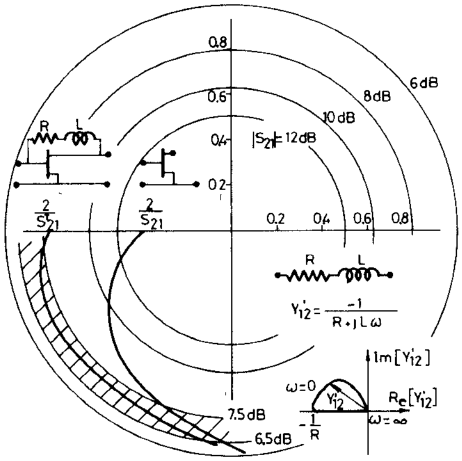


Fig. 5. Feedback diagram for equalization and matching. Example for RL feedback circuit.

and

$$\frac{S_{12}^T}{S_{21}^T} \simeq \frac{Y_{12}+Y_{12}'}{Y_{21}} \tag{7.d}$$

where we have made the same approximations that lead to (1) and (2), for S_{21} of the transistor reasonably high.

In a complex plane, constant S_{21}^T curves are a family of circles centered at the origin, whose radii are $2/|S_{21}^T|$, as shown in Fig. 4. We plot in the diagram typical values of $2/S_{21}$, $2\,S_{11}/S_{21}$, and $2\,S_{22}/S_{21}$ for different frequencies in the band of interest. The term Y_{12}' represents a vector translation. Therefore the problem is to find out the type of feedback circuit that translates the $2/S_{21}$ curve into a constant $|S_{21}^T|$ circle, placing $2\,S_{11}^T/S_{21}^T$ and $2\,S_{22}^T/S_{21}^T$ near to the center of the diagram. This is easy for an experienced circuit designer. This graphical method gives the topology and initial values for the feedback circuit. Figs. 4, 5 illustrate this procedure for two simple cases, one for a parallel resistance whose effect is a pure frequency independent translation, and the second which includes an inductor whose effect is to decrease the Y_{12}' value for high frequencies which produces gain equalization. In Section III we shall show a practical example. This method is also applicable to series feedback, changing Y_{ij}' for Z_{ij}' in (7).

III. Application I: Transistor Neutralization

A high frequency transistor normally operates in the proximity of its f_T with the gain decreasing at about 6 dB per octave, with increasing internal feedback, S_{12}. One means of increasing gain and reducing S_{12} in a tuned amplifier is by use of a parallel feedback network.

In Fig. 6(a) we have plotted the feedback diagrams for the BFT-75 transistor working at 1 GHz (f_T=4 GHz), V_{CE}=5 V, I_C=10 mA. Point A corresponds to the transistor alone (Y_{12}'=0) which has a gain G=11.12 dB and a stability factor K=1.054. Using a feedback inductance we can get greater gain (point B). This solution may however produce instability at low frequencies.

We can obtain the same effect adding a section of line to the collector and using a capacitor as feedback element. Moreover, this solution isolates the collector and base terminals from each other on a dc voltage basis.

The new family of curves-transistor plus section of line are plotted in Fig. 6(b). We can translate point D (no

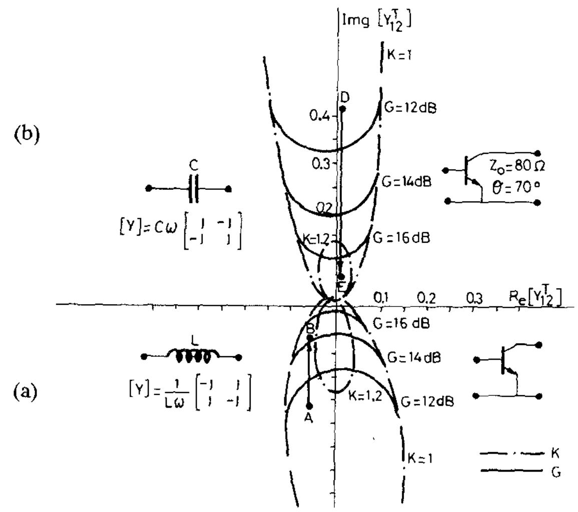


Fig. 6. Feedback diagrams for the Siemens BFT-75 transistor (a) and transistor plus section of line (b).

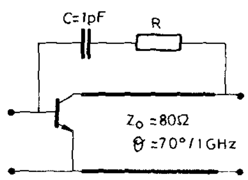


Fig. 7. Neutralized transistor configuration.

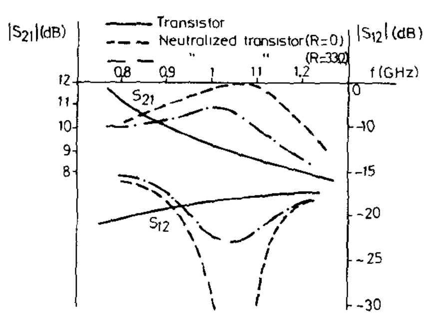


Fig. 8. Measured results for neutralized transistor.

TABLE I
NEUTRALIZED AMPLIFIER RESULTS

	R(Ω)	G_{max}(dB)	G_i (dB)
Transistor	-	11.2	-15
Feedback	-	16.9	-35
	12	15.9	-25
	33	13.5	-20

feedback) to point E using a capacitor $C=1$ pF, obtaining graphically a gain $G=17$ dB and a stability factor of $K=1.25$. Exact computation gives $G=16.56$ dB and $K=1.28$ which confirms the validity of the graphical construction.

To avoid unstability at higher frequencies we insert a small resistance R in the feedback circuit as indicated in Fig. 7.

The measured S-parameters for the transistor alone and the neutralized transistor are plotted in Fig. 8, where good neutralization and increase in gain are observed. Finally the amplifier was tuned with external stubs obtaining the results listed in Table I.

IV. Application II: Broad-Band Medium Power MESFET Amplifiers

Power MESFET are high Q devices and conditionally stable over part of their usual frequency range. Therefore, it's difficult to equalize gain with low VSWR in bandwidths greater than 10 percent as our previous experience, shows in a no-feedback design [8] which required a lot of computer work. Using parallel feedback it is relatively easy to obtain flat gain, lowering the input and output reflection coefficients in addition to making the device unconditionally stable.

In this application we use the MESFET NE 464194 device. Its measured S-parameter and calculated stability factor K are listed in Table II at three frequencies in the 3.7–4.2-GHz band. ($V_{DS}=7$ V, $I_D=120$ mA).

It is evident that the transistor is conditionally stable and it has high reflection coefficients.

In Fig. 9 we have plotted the transistor feedback diagrams at the frequencies listed above. These diagrams include input and output 5-mm sections of 50-Ω line needed to connect the feedback network.

With the vector translations indicated in the diagrams we can obtain a constant $G_{max} \simeq 11.5$ dB and make the device stable, $K>1$. Note that Y_{12}' is a vector of nearly constant magnitude and rotates in clockwise direction when increasing frequency. We can obtain this behavior with several types of circuits. However, the necessity of controlling feedback for frequencies out of the required bandwidth, together with certain physical assembly requirements related to the transistor package, reduce the possibilities. We finally chose the circuit shown in Fig. 10, which also shows the Y_{12}' variation with frequency. Note that this type of network permits a translation in any direction on the complex plane, which makes it a very useful and convenient feedback circuit. The initial values obtained

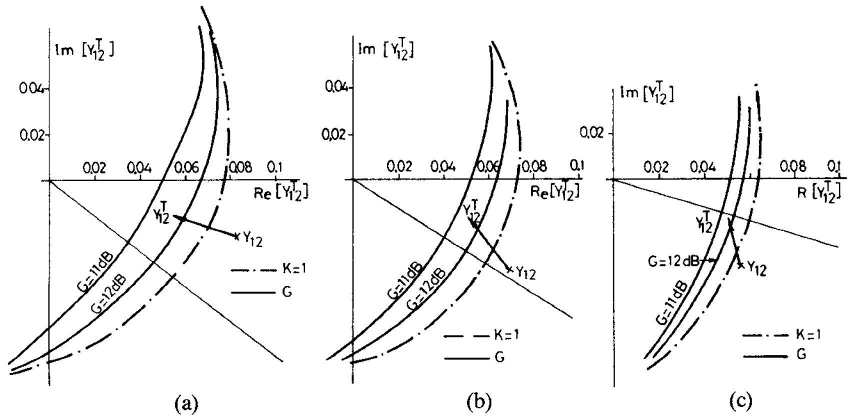


Fig. 9. Feedback diagrams for the Nippon Electric Company 464194 transistor. (a) 3.7 GHz. (b) 3.95 GHz. (c) 4.2 GHz.

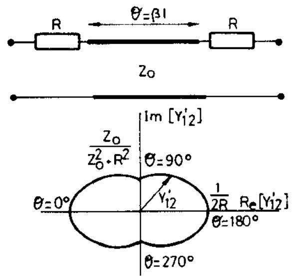


Fig. 10. Schematic of feedback circuit showing Y_{12} variation with frequency.

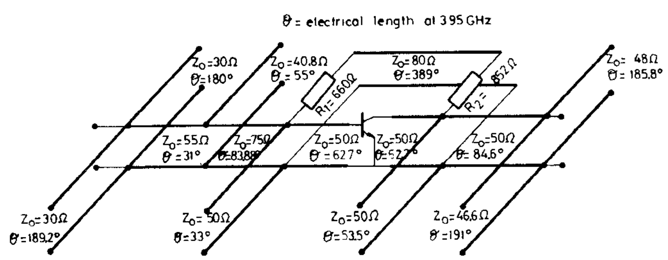


Fig. 11. Complete amplifier stage including feedback circuit, input, and output matching networks.

TABLE II
S-Parameters and K Factor of NE-464194 Transistor

f(GHz)	S_{11}	Φ_{11}	S_{12}	Φ_{12}	S_{21}	Φ_{21}	S_{22}	Φ_{22}	K
3.700	0.897	-156.1	0.053	-12.4	1.579	60.6	0.489	-117.1	0.637
3.950	0.897	-158.1	0.055	-18.8	1.541	43.1	0.556	-121.6	0.560
4.200	0.908	-157.1	0.058	-20.2	1.556	37.4	0.584	-120.4	0.464

TABLE III
S-Parameters K Factor and G_{max} of Feedback NE 464194 Transistor

f (GHz)	S_{11}	S_{12}	S_{21}	S_{22}	K	G_{max} (dB)
3.70	0.825	0.038	1.510	0.472	1.887	10.51
3.95	0.822	0.046	1.460	0.529	1.627	10.28
4.20	0.823	0.050	1.449	0.555	1.426	10.75

from the diagrams were

$$R=750\ \Omega$$
$$Z_0=80\ \Omega$$
$$\theta=395° \text{ (at 3.95 GHz)}$$
$$G\simeq 11.5 \text{ dB}$$
$$K>1.35.$$

The exact calculations are listed in Table III (phases are omitted for the sake of simplicity).

Compared to the values given in Table II we can see that the feedback MESFET is unconditionally stable, the gain is almost constant and the reflection coefficients lower. Finally we proceed to the design of input and output matching networks. Some graphic work on the Smith chart, followed by computer optimization [9], leads to the amplifier stage whose schematic is indicated in Fig. 11.

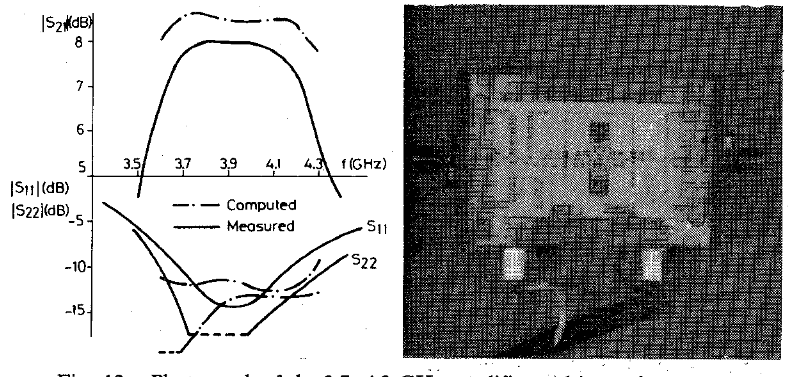


Fig. 12. Photograph of the 3.7–4.2-GHz amplifier and its performance.

Fig. 12 shows a view of the assembled amplifier with the measured gain and reflection coefficients. Decrease in gain and improvement in reflection coefficients are due at least partly to the losses in the thick-film microstrip lines.

We have shown how the graphical method can be applied to the design of communications MESFET amplifiers. We must emphasize that computer optimization was done only in the final stage on a model that was close enough to the final circuit so that time and money spent was considerably reduced.

V. Application III: Very Broad-Band (0.1–12 GHz) Matched Transistor Amplifier

We shall now apply the basic theory above described to the design of a matched MESFET amplifier from 0.1 to 12 GHz. We use a commercially available transistor NE-38800 (Chip on ≠74124A carrier) biased to $V_{DS}=3$ V, $I_D=30$ mA, using the S-parameters given in data sheets.

We plotted in Fig. 13 functions $2/S_{21}$, $2S_{11}/S_{21}$, and $2S_{22}/S_{21}$. From a graphical inspection we can see that a parallel feedback resistance tends to match the transistor but a strong feedback $Y_{12}'=-0.6$ is needed, which makes the gain very low. In fact, as other authors [3], [5] have mentioned this occurs with low transconductance devices such as high frequency MESFET. This effect can be avoided using two transistor in a parallel configuration which increases the transconductance.

In Fig. 14 (a) we have plotted the above functions for the parallel transistor configuration. It can be seen that a parallel feedback resistance, $Y_{12}'=-0.3$, tends to adapt the device but gain is still low for frequencies higher than 5 GHz.

It should be noted that for points of the $2/S_{21}$ curve located in the third quadrant, the parallel resistance produces a negative feedback while for points in fourth quadrant will give a positive feedback. Therefore, it would be desirable if the high-frequency part on the $2/S_{21}$ curve–low $|S_{21}|$–(were located in the fourth quadrant while the low-frequency points remain still in the third one. This can be easily done by a counterclockwise rotation of the $2/S_{21}$ curve, which can be accomplished with a short transmission line section or an inductance in the drain port. This effect is illustrated in Fig. 14 (b) for the case of a 0.5-nH inductance. Note also that curve $2S_{22}/S_{21}$ is displaced to the right decreasing the output reflection. Considering now

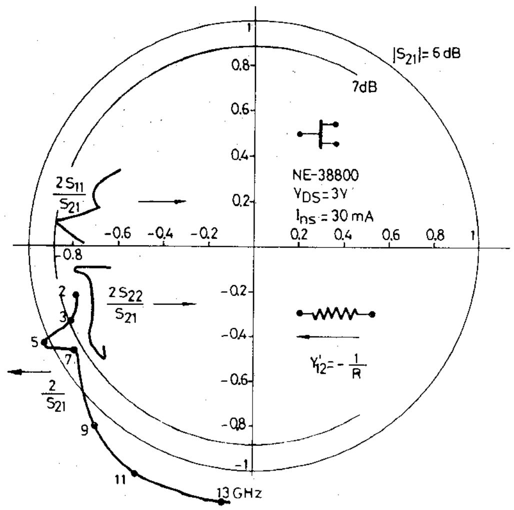


Fig. 13. S-parameter feedback diagram for the Nippon Electric Company NE 38800 transistor showing the effect of a parallel resistance.

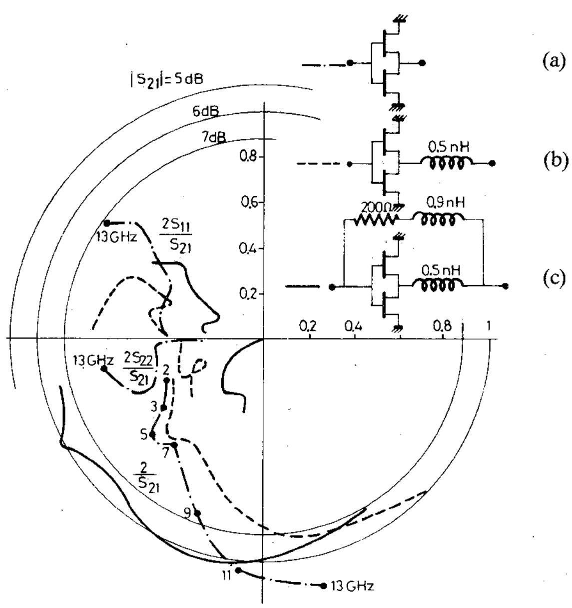


Fig. 14. Graphical construction for (a) parallel transistor cell; (b) cell plus series inductance; and (c) complete feedback configuration.

the feedback network, it can be seen, from Fig. 14, that a simple vector translation ($Y_{12}'=-0,4$) displaces the $2/S_{21}$ (b) curve to a region between 6 and 7 dB constant $|S_{21}|$

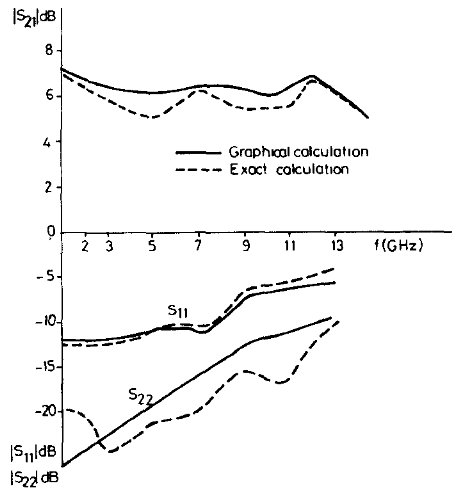


Fig. 15. Exact computed (broken line) and graphically calculated (full line) S-parameters for the feedback configuration.

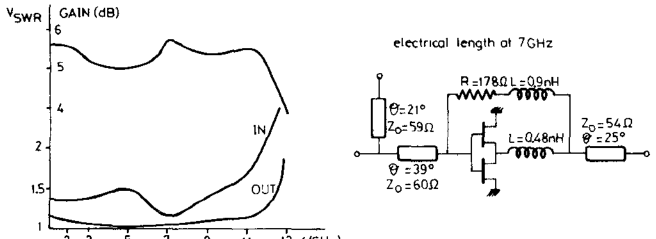


Fig. 16. Computed gain and VSWR of the 0.1–12-GHz amplifier.

circles, obtaining, in this way a good equalization except in the high frequency points. This effect is corrected by adding a series feedback inductance. Corrected values of the feedback circuit are calculated using expressions (A.11) (Appendix II) giving a 200-Ω resistence and a 0.9-nH inductance. Note also that a substantial improvement in reflection coefficients is obtained.

Using the exact expressions, (A.9) network parameters were recalculated and results are plotted in Fig. 15. It can be seen that exact calculations give slightly lower gain, as was expected, but graphical values are very close to the exact ones. Finally, two simple matching networks were designed and the complete circuit was optimized by computer [9] resulting in the final configuration and results shown in Fig. 16. Stability factor was calculated, obtaining $K>1$ for all frequencies in the band.

VI. Conclusion

A graphical procedure for the design of feedback transistor amplifiers has been described. Feedback diagrams based upon constant stability ellipses, constant $G_{\max}$ circles and constant $|S_{21}|$ circles have been plotted, explaining the construction rules and formulas. We have shown how easy it is to find the appropriate feedback circuit values using the graphical method.

As a first and simple application of this method, a neutralized bipolar transistor amplifier has been developed. We have shown that for transistor working near f_T, a substantial increase in gain and neutralization is achieved and the graphical method makes the design very easy. A feedback stage was constructed using a BFT-75 transistor tuned to 1 GHz obtaining a 16-dB gain–5-dB increase with a 10-dB improvement in S_{12}. This technique in very useful for cascadable tuned amplifiers.

The graphical method has been then applied to the design of a 3.7–4.2-GHz medium power MESFET amplifier stage. A versatile feedback network has been found consisting of two resistances joined together by a transmission line, whose values are calculated using the feedback diagrams. An amplifier stage was constructed using a NE464194 MESFET and thick-film microstrip circuitry. We have obtained a 8 ± 0.3-dB gain, with excellent stability ($K>1.35$) and low VSWR, for an output power of 180 mW. It should be noted that these transistors are high Q and unstable devices in the frequency range complicating its matching and gain equalization using conventional techniques. Our method has proved to be easy and useful to solve these problems.

Finally, an ultrawide-band MESFET amplifier stage has been designed using constant $|S_{21}|$ feedback circles, showing how graphical techniques allow finding the type of feedback circuit and calculating the network parameters so closely that a single computer optimization leads to the final network values. Using a NE-38800 MESFET chip we have designed a feedback amplifier with 5.5-dB gain in a 0.1 to 12-GHz frequency band and low reflection parameters ($|S_{11}|<-10$ dB, $|S_{22}|<-13$ dB in the full band).

The graphical method we have described is, then, an important tool to the design of feedback microwave transistor amplifiers.

Appendix I

A. Constant Stability Factor K_T Curves

The Rollet's stability factor K_T of the circuit shown in Fig. 1 is given by

$$K_T=\frac{2g_{11}\cdot g_{22}-\mathrm{Real}\left[Y_{21}\cdot Y_{12}^T\right]}{|Y_{21}\cdot Y_{12}^T|} \tag{A.1}$$

with $g_{ii}=\mathrm{Real}\,(Y_{ii})$ and $Y'_{ij}\ll Y_{ij}$ except Y'_{12}.

Expression (A.1) can be written as

$$K_T=\frac{A}{Y_{12}^T}-\cos\theta \tag{A.2}$$

where

$$A=\frac{2g_{11}\cdot g_{22}}{|Y_{21}|} \tag{A.3}$$

$$\theta=\varphi_{21}+\varphi_{12}^T \text{ with } \varphi_{ij}=\arg(Y_{ij}). \tag{A.4}$$

By taking $Y_{12}^T\cdot e^{j\varphi_{21}}$ as a variable and substituting $Y_{12}^T\cdot e^{j\varphi_{21}}=u+jv$ (A.4), expression (A.2) may be written as

$$K_T=\frac{A}{\sqrt{u^2+v^2}}-\frac{v}{\sqrt{u^2+v^2}}. \tag{A.5}$$

After some algebra we can transform (A.5) into a more familiar expression

$$\frac{(u+A/M)^2}{K_T^2\cdot A^2/M^2}+\frac{v^2}{A^2/M}=1 \tag{A.6}$$

with $M=K_T^2-1$.

Taking u and v as Cartesian coordinates in a complex plane, expression (A.6) is a family of ellipses whose centers are on the real axis $(-A/(K_T^2-1),0)$ and the axis lengths are given by $K_T \cdot A/(K_T^2-1)$ and $A/(K_T^2-1)^{1/2}$.

In fact, taking Y_{12}^T as a variable the resultant family of curves will be those given by (A.6) rotated an angle φ_{21} in a clockwise direction such as indicated in Fig. 2.

B. Constant Gain $G_{\max}$ Curves

The maximum available gain of the feedback amplifier shown in Fig. 1 can be expressed as

$$G_{\max} = \frac{|Y_{21}|}{|Y_{12}^T|}\left[K_T - \sqrt{K_T^2 - 1}\right], \qquad \text{for } K_T > 1 \tag{A.7}$$

where the approximations $Y'_{ij} \ll Y_{ij}$ except Y'_{12} are retained.

Expression (A.7) can be written as

$$\frac{G_{\max}^2 |Y_{12}^T|^2}{|Y_{21}|^2} - \frac{2K_T G_{\max}|Y_{12}^T|}{|Y_{21}|} = -1.$$

Using transformations given by (A.2), (A.3), and (A.4) we can write

$$\left(u + \frac{|Y_{21}|}{G_{\max}}\right)^2 + v^2 = \frac{2 \cdot A|Y_{21}|}{G_{\max}} \tag{A.8}$$

which is a family of circles centered at $(0, -|Y_{21}|/G_{\max})$ with radii $(2A|Y_{21}|/G_{\max})^{1/2}$. The actual circles are rotated an angle φ_{21} in a clockwise direction such as indicated in Fig. 3.

Appendix II

The total S_{11}^T and S_{21}^T parameters of the feedback transistor shown in Fig. 1 can be expressed as [10]

$$S_{11}^T = \left[(1 - Y_{11} - Y'_{11}) \cdot (1 + Y_{22} + Y'_{22}) + (Y_{12} + Y'_{12})Y_{21}\right]\frac{1}{\Delta} \tag{A.9.a}$$

$$S_{21}^T = -2Y_{21}/\Delta \tag{A.9.b}$$

$$S_{12}^T = \frac{-2(Y_{12} + Y'_{12})}{\Delta} \tag{A.9.c}$$

and

$$S_{22}^T = \left[(1 + Y_{11} + Y'_{11})(1 - Y_{22} - Y'_{22}) + (Y_{12} + Y'_{12})Y_{21}\right]\frac{1}{\Delta} \tag{A.9.d}$$

with $\Delta = (1 + Y_{11} + Y'_{11})(1 + Y_{22} + Y'_{22}) - (Y_{12} + Y'_{12})$. Y_{21}, and only the $Y'_{21} \ll Y_{21}$ approximation has been made.

Expressions (A.9.a) and (A.9.b) can be written in a different way, i.e.,

$$\frac{2S_{11}^T}{S_{21}^T} = \frac{2S_{11}}{S_{21}} - Y'_{12} + \frac{Y'_{11}(1 + Y_{22}) - Y'_{22}(1 - Y_{11}) + Y'_{11}Y'_{22}}{Y_{21}} \tag{A.10.a}$$

and

$$\frac{2}{S_{21}^T} = \frac{2}{S_{21}} + Y'_{12} - \frac{Y'_{11}(1 + Y_{22}) + Y'_{22}(1 + Y_{11}) + Y'_{11}Y'_{22}}{Y_{21}} \tag{A.10.b}$$

and similar expressions for the other two parameters.

The term $Y'_{11}Y'_{22}/Y_{21}$ is negligible. Furthermore, in the case of a feedback network of a series type (RL, RC) $Y'_{11} = Y'_{22} = -Y'_{12}$ in which case expressions (A.10) can be written as

$$\frac{2S_{11}^T}{S_{21}^T} = \frac{2S_{11}}{S_{21}} - Y'_{12}\left[1 - \frac{Y_{11} + Y_{22}}{Y_{21}}\right] \tag{A.11.a}$$

and

$$\frac{2}{S_{21}^T} = \frac{2}{S_{21}} + Y'_{12}\left[1 + \frac{2 + Y_{11} + Y_{22}}{Y_{21}}\right] \tag{A.11.b}$$

and similar expressions for the other parameters.

Returning to expressions (A.9) a rough approximation can be made (if $Y'_{11} \ll Y_{11}$, $Y'_{22} \ll Y_{22}$ and both much less than Y_{21}) that leads directly to expressions (7) given in the text. These approximations are good ones for bipolar transistors and fairly good ones for a first step in graphical design for FET's. However, for FET's (A.10) and (A.11) should be used in a final correction step much as indicated in the text.

Acknowledgment

The authors wish to thank A. Delgado for his helpful comments and aid in computer work. Thanks are also due to people from the Centro de Investigaciones y Estudios (CTNE) for supporting facilities in the construction of power MESFET amplifier.

References

[1] J. B. Coghlin, R. J. Gelsing, and H. J. Van-Der-Leak, "A monolithic silicon wideband amplifier from Dc to 1 GHz," *IEEE J. Solid-State Circuits*, Dec. 1973.

[2] F. Pérez and V. Ortega, "Diseño de amplificadores encadenados. Aplicación en CATV en la banda 40-860 MHz," *Mundo Electrónico*. pp. 123–128, Sept. 1980.

[3] E. Ulrich, "Use negative feedback to slash wideband VSWR," *Microwaves*, pp. 66–70, Oct. 1978.

[4] A. K. Gupta, J. A. Higging and D. R. Decker, "Progress in broad-band GaAs monolithic amplifier," in *Int. Electron Devices Meeting, Tech. Dig.*, pp. 269–272, Dec. 1979.

[5] K. B. Niclas "GaAs MESFET feedback amplifier. Design considerations and characteristics," *Microwave J.* pp. 39–48, Mar. 1981.

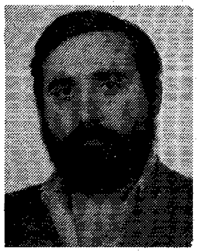
[6] S. E. Sussman-Fort, "Computer-simulated design of an active microwave all-pass network," *IEEE Trans. Microwave Theory Tech.* pp. 1023–1025, Dec. 1979.

[7] P. Grivet, *Microwave Circuits and Amplifiers.* London, England: *Academic*, 1976, Ch. 8.

[8] A. Delgado, A. Velasco, and V. Ortega, "Amplificador lineal de potencia media con MESFET para radioenlaces in la banda 3.7–4.2 GHz," presented at I Symposium Nacional del Comité Español de la URSI, Oct. 1980.

[9] A. Delgado and F. Pérez, "ALFIL: Un programa de análisis y optimización de circuitos de microondas," Internal Rep. Microwave Dep.

[10] "S-parameters, circuit analysis and design," Hewlett Packard, Application Note 95.



Felix Perez received the Ingeniero de Telecomunicación degree from the Politechnic University of Madrid in 1977.

He is presently working toward the Ph. D. degree on microwave feedback solid-state circuits from the Politechnic University of Madrid. He is an assistant Professor in the Microwave Department and has held a research fellowship from the Ministerio de Universidades e Investigación. He has been engaged in the development of CATV amplifiers.

Vicente Ortega received the Ingeniero de Telecomunicación degree from Politechnic University of Madrid in 1967, the M.S. degree in electrical engineering from Stanford University, CA, in 1969, and Ph. D. degree from Politechnic University of Madrid in 1972.

He was appointed a Professor at the Microwave Department and has been engaged in microwave solid-state circuit work. He is now Head of the Microwave Department where its actual interests include MESFET amplifiers and oscillators, fused-silica microwave circuits and high frequency front-ends for TV receivers.

Matching Network Design Studies for Microwave Transistor Amplifiers

GEORGE P. YOUNG, MEMBER, IEEE, AND SEAN O. SCANLAN, FELLOW, IEEE

Abstract—**Several techniques for design of microwave amplifiers using lumped-element and distributed matching networks are discussed. An extension to the Remez-algorithm design approaches is proposed, whereby gain and ripple quantities may be adjusted using a numerical optimization procedure in order to achieve complete absorption of device model elements and also impedance transformation.**

I. Introduction

In designing microwave transistor amplifiers, a widely used technique is that of modeling the active device in terms of simple input and output networks with a gain–slope parameter and subsequently designing matching networks incorporating the model elements and having an inverse gain–frequency slope, e.g., [1]–[4]. Departures from a flat response are caused by a) modeling inaccuracies in output and input admittances, b) the use of a unilateral approximation (see [5]), and c) due to imperfections in the matching network responses. It is usual that computer optimization be used to refine an initial design.

Modeling networks (and gain–bandwidth restrictions which may be derived) are discussed in Section II, with matching network design being treated in Section III. Results are presented in Section IV and conclusions are presented in Section V.

Throughout the discussion, four devices are considered for the purposes of illustration. These are a) the HP 1-μm gate packaged device (FET) [1], b) the Plessey COD package device [2], the HP bipolar device [3], and the HP 1-μm chip device [6]. S-parameter data (50-Ω reference) is given in Table I(a)–(d). Calculation of stability quantities K and B_1 ([7]) indicates that all devices are unconditionally stable within the frequency ranges for which data are available,

Manuscript received July 28, 1980; revised March 16, 1981.
G. P. Young was with the Department of Electrical and Electronic Engineering, University College, Dublin, Ireland. He is now with Telectron Ltd., Tallaght, Co. Dublin, Ireland.
S. O. Scanlan is with the Department of Electrical and Electronic Engineering, University College, Dublin 2, Ireland.

0018-9480/81/1000-1027$00.75 ©1981 IEEE

TABLE I
S-PARAMETER DATA FOR TRANSISTORS a)–d)

FREQUENCY	$\lvert S_{11}\rvert$	$\lvert S_{12}\rvert$	$\lvert S_{21}\rvert$	$\lvert S_{22}\rvert$	$\angle S_{11}$	$\angle S_{12}$	$\angle S_{21}$	$\angle S_{22}$
4.0 GHz	0.712	0.036	2.589	0.563	-129.0	25.9	74.7	- 42.4
4.5 GHz	0.741	0.038	2.484	0.520	-148.6	20.3	63.1	- 47.9
5.0 GHz	0.682	0.038	2.375	0.485	-161.7	16.7	51.6	- 55.8
5.5 GHz	0.695	0.040	2.229	0.457	-177.2	12.6	38.9	- 64.0
6.0 GHz	0.668	0.043	2.111	0.412	168.1	6.9	26.9	- 74.7
6.5 GHz	0.712	0.045	1.987	0.370	152.4	0.3	15.3	- 83.3
7.0 GHz	0.659	0.047	1.810	0.320	145.2	-5.0	5.3	- 95.9
7.5 GHz	0.695	0.048	1.698	0.266	135.7	-11.0	- 6.4	-109.9
8.0 GHz	0.674	0.050	1.649	0.244	126.7	-16.8	-16.1	-132.0

(a)

FREQUENCY	$\lvert S_{11}\rvert$	$\lvert S_{12}\rvert$	$\lvert S_{21}\rvert$	$\lvert S_{22}\rvert$	$\angle S_{11}$	$\angle S_{12}$	$\angle S_{21}$	$\angle S_{22}$
8.0 GHz	0.620	0.066	1.190	0.880	- 64.0	134.0	150.0	-30.0
9.0 GHz	0.460	0.089	1.340	0.840	- 87.0	129.0	140.0	-43.0
10.0 GHz	0.410	0.082	1.220	0.820	- 96.0	138.0	130.0	-38.0
11.0 GHz	0.400	0.082	1.090	0.830	-116.0	138.0	125.0	-45.0
12.0 GHz	0.250	0.087	1.110	0.860	-107.0	154.0	120.0	-42.0

(b)

FREQUENCY	$\lvert S_{11}\rvert$	$\lvert S_{12}\rvert$	$\lvert S_{21}\rvert$	$\lvert S_{22}\rvert$	$\angle S_{11}$	$\angle S_{12}$	$\angle S_{21}$	$\angle S_{22}$
1.0 GHz	0.670	0.060	3.200	0.350	160.0	62.0	72.0	- 78.0
1.25 GHz	0.675	0.080	2.700	0.350	154.0	63.0	66.0	- 81.0
1.5 GHz	0.680	0.100	2.200	0.350	147.0	63.0	60.0	- 85.0
1.75 GHz	0.068	0.120	1.880	0.350	140.0	63.0	54.0	- 89.0
2.0 GHz	0.680	0.130	1.570	0.350	134.0	63.0	48.0	- 93.0
2.25 GHz	0.685	0.140	1.490	0.350	128.0	62.0	45.0	- 98.0
2.5 GHz	0.690	0.150	1.260	0.360	122.0	61.0	41.0	-103.0

(c)

FREQUENCY	$\lvert S_{11}\rvert$	$\lvert S_{12}\rvert$	$\lvert S_{21}\rvert$	$\lvert S_{22}\rvert$	$\angle S_{11}$	$\angle S_{12}$	$\angle S_{21}$	$\angle S_{22}$
8.0 GHz	0.719	0.038	1.887	0.618	253.8	54.9	99.4	317.4
9.0 GHz	0.712	0.038	1.720	0.623	248.8	56.3	92.0	313.1
10.0 GHz	0.708.	0.038	1.510	0.625	242.2	57.8	85.5	309.3
11.0 GHz	0.705	0.038	1.400	0.627	238.7	59.2	81.7	306.0
12.0 GHz	0.709	0.038	1.310	0.622	235.2	60.6	77.7	304.0

(d)

(a) Transistor a)

(b) Transistor b)

(c) Transistor c)

(d) Transistor d)

with the exception of device b at the lower end of the range.

II. MODELING NETWORKS AND GAIN–BANDWIDTH LIMITATIONS

A. Gain Relations

The circuit to be considered consists of the transistor connected to the terminations by lossless matching networks, as shown in Fig. 1. With S-parameters and reflection coefficients normalized to the same reference (conventionally 50 Ω) the transducer power gain is given by [7]

$$G_T = \frac{|S_{21}|^2\left(1-|S_g|^2\right)\left(1-|S_L|^2\right)}{|1-S_gS_{11}-S_LS_{22}+S_gS_L\Delta|^2}, \qquad \Delta = S_{11}S_{22}-S_{12}S_{21}. \tag{1}$$

A convenient approximation for design purposes is to set

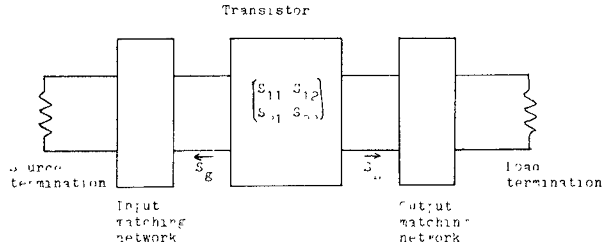


Fig. 1. Amplifier configuration under discussion.

S_{12} equal to 0 with other parameters unchanged. Thus one may write

$$G_u = G_T|_{S_{12}=0} = \underbrace{\frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)}}_{\text{(term 1)}} \cdot \underbrace{\frac{\left(1-|S_{11}|^2\right)\left(1-|S_g|^2\right)}{|1-S_gS_{11}|^2}}_{\text{(term 2)}} \cdot \underbrace{\frac{\left(1-|S_{22}|^2\right)\left(1-|S_L|^2\right)}{|1-S_LS_{22}|^2}}_{\text{(term 3)}} \tag{2}$$

where the first term is $G_{u\max}$, obtained when the ports are conjugately terminated with $S_{12}=0$, and terms 2 and 3 are transducer gains of input and output networks terminated in S_{11} and S_{22}, respectively. The device properties are ordinarily such that $G_{u\max}$ falls with frequency at a rate of about 6 dB per octave and hence to achieve broad-band flat gain it is necessary to design input and output networks so that the product of terms 2 and 3 in (2) gives an inverse gain–frequency slope.

B. Modeling Considerations

It is essential to have simple models for immittance quantities associated with S_{11} and S_{22}, and the elements in these models must be capable of absorption into matching networks. Modeling networks of simple structure using lumped elements and alternatives using commensurate-distributed elements are shown in Fig. 2. (see, e.g., [1], [3]). In the case of commensurate distributed lines, 1/4 wave frequencies of $f_0 = 1.5f_H$ and $f_0 = 2f_H$ were chosen, where f_H is the highest in-band frequency. Element values were calculated for the devices under study using "average," least square, or optimization-based fitting techniques as appropriate. It is noted that the FET chip device could be adequately modeled using RC networks, but inclusion of inductive elements was necessary for packaged FET or bipolar devices. A similar statement applies in the case of the commensurate networks using the concept of capacitors and inductors with the transformed frequency variable.

C. Gain–Bandwidth Considerations

Gain–bandwidth studies may be undertaken for the models obtained. These studies are of interest in that they